IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor memory device comprising:

a plurality of word lines formed along a first direction;

a plurality of bit lines formed along a second direction crossing at right angles to the first direction;

a first memory cell including a magneto-resistive element which has either a first resistance or a second resistance smaller than the first resistance;

a second memory cell including a magneto-resistive element which has a resistance between the first and second resistances;

a memory cell array including the first and second memory cells disposed [[in]] at intersections of ~~the~~ a word line and bit [[line]] lines;

a row decoder which selects the word line;

a row driver including a first current source configured to supply a first write current to the word line selected by the row decoder and a second current source configured to supply a second write current ~~which supplies a first write current~~ to the word line selected by the row decoder, an absolute value of the second write current being smaller than that of the first write current, the first current source supplying the first write current to the word line such that the magneto-resistive element of the first memory cell has either the first or second resistance to perform a write operation, and the second current source supplying the second write current to the word line such that the magneto-resistive element of the second memory cell has a resistance between the first and second resistances;

a column decoder which selects [[the]] a bit line;

a column driver which supplies a ~~second~~ third write current to the bit line selected by the column decoder; and

a sense amplifier which amplifies data read from the first memory cell selected by the row decoder and column decoder.

Claims 2-4 (Canceled).

Claim 5 (Currently Amended): The device according to claim [[4]] 1, further comprising:

a hold circuit which holds the value of the ~~first~~ second write current required to set the resistance of the magneto-resistive element of the second memory cell to a value between the first and second resistances.

Claim 6 (Canceled).

Claim 7 (Currently Amended): ~~The~~ A semiconductor device ~~according to claim 6, wherein~~ comprising:

a plurality of word lines formed along a first direction;

a plurality of bit lines formed along a second direction crossing at right angles to the first direction;

a first memory cell including a magneto-resistive element which has either a first resistance or a second resistance smaller than the first resistance;

a second memory cell including a magneto-resistive element which has a resistance between the first and second resistances;

a memory cell array including the first and second memory cells disposed at intersections of a word line and bit lines;

a row decoder which selects the word line;

a row driver configured to supply a first write current to the word line selected by the row decoder;

a column decoder configured to select a bit line;

a column driver including a first current source which ~~the column driver~~ supplies ~~the~~ a second write current to the bit line such that the magneto-resistive element of the first memory cell has either the first or second resistances to perform a write operation[[,]] and a second current source which ~~the column driver~~ supplies ~~the second~~ a third write current to the bit line such that the magneto-resistive element of the second memory cell has a resistance between the first and second resistances, an absolute value of the third write current being smaller than that of the second write current; and

a sense amplifier configured to amplify data read from the first memory cell selected by the row decoder and column decoder.

Claim 8 (Currently Amended): The device according to claim 7, further comprising:

a hold circuit which holds the value of the ~~second~~ third write current required to set the resistance of the magneto-resistive element of the second memory cell to a value between the first and second resistances.

Claim 9 (Original): The device according to claim 1, wherein the second memory cells are arranged at the intersection of any one bit line and word lines.

Claim 10 (Original): The device according to claim 1, wherein the sense amplifier amplifies the data read from the first memory cell based on the data held by the second memory cell.

Claim 11 (Original): The device according to claim 10, wherein the sense amplifier identifies the data read from the first memory cell by a magnitude with respect to the data read from the second memory cell.

Claim 12 (Original): The device according to claim 1, further comprising:

a judgment circuit to judge whether or not the resistance of the magneto-resistive element of the second memory cell is in a predetermined range between the first and second resistances; and

a control circuit to command the rewriting of the data with respect to the second memory cell, when the resistance of the magneto-resistive element of the second memory cell is not in a predetermined range as a result of judgment in the judgment circuit.

Claim 13 (Original): The device according to claim 12, wherein the control circuit controls the value of the current supplied by either one of the row driver and column driver in accordance with a judgment result in the judgment circuit in commanding the rewriting.

Claim 14 (Currently Amended): A semiconductor memory device comprising:

a plurality of word lines formed along a first direction;

a plurality of bit lines formed along a second direction crossing at right angles to the first direction;

a memory cell including a magneto-resistive element;

a memory cell array including [[the]] memory cells disposed [[in]] at an intersection of [[the]] a word line and bit [[line]] lines;

a row decoder which selects the word line;

a column decoder which selects [[the]] a bit line;

a driver circuit which supplies write currents to the word line and bit line selected by the row decoder and column decoder, respectively and in which a current value of the write current is variable in accordance with the word line or bit line, the driver circuit including a first current source and a second current source, the first current source supplying the write current, the second current source supplying the write current and having a greater current drive ability than the first current source; and

a sense amplifier which amplifies data read from the memory cell selected by the row decoder and column decoder.

Claim 15 (Currently Amended): The device according to claim 14, wherein the ~~driver circuit comprises a~~ first current source is provided for each of the word lines, and [[a]] the second current source is provided for each of the word lines ~~and having a greater current drive ability than the first current source~~.

Claim 16 (Original): The device according to claim 15, wherein the second current source supplies the write current to the word line such that the magneto-resistive element of the memory cell has either a first resistance or a second resistance smaller than the first resistance to perform write operation, and

the first current source supplies the write current to the word line such that the magneto-resistive element of the memory cell has a resistance between the first and second resistances.

Claim 17 (Original): The device according to claim 16, wherein the memory cells having the resistance between the first and second resistances are arranged at intersections of any one bit line and word lines.

Claim 18 (Original): The device according to claim 16, wherein the sense amplifier amplifies the data read from the memory cell having either the first or second resistance based on the data held by the memory cell which has a resistance between the first and second resistances.

Claim 19 (Original): The device according to claim 18, wherein the sense amplifier identifies the data read from the memory cell having either the first or second resistance by a magnitude with respect to the data read from the memory cell which has the resistance between the first and second resistances.

Claim 20 (Original): The device according to claim 16, further comprising:

a hold circuit which holds the value of the write current required to set the resistance of the magneto-resistive element of the memory cell to a value between the first and second resistances.

Claim 21 (Original): The device according to claim 16, further comprising:

a judgment circuit to judge whether or not the resistance of the magneto-resistive element of the memory cell is in a predetermined range between the first and second resistances; and

a control circuit to command the rewriting of the data with respect to the memory cell, when the resistance of the magneto-resistive element of the memory cell is not in the predetermined range as a result of judgment in the judgment circuit.

Claim 22 (Original): The device according to claim 21, wherein the control circuit controls the value of the current supplied by the driver circuit in accordance with a judgment result in the judgment circuit in commanding the rewriting.

Claim 23 (Currently Amended): The device according to claim 14, wherein the ~~driver circuit~~ second current source supplies the write current to the bit line such that the magneto-resistive elements of the memory cells arranged at the intersections of the word lines and some of the bit lines have either a first resistance or a second resistance smaller than the first resistance to perform write operation, and the ~~driver circuit~~ first current source supplies the write current to the bit line such that the magneto-resistive elements of the memory cells arranged at the intersections of the word lines and the remaining bit lines have a resistance intermediate between the first and second resistances.

Claim 24 (Original): The device according to claim 23, wherein the memory cells having the resistance between the first and second resistances are disposed in an intersection of any one bit line and word lines.

Claim 25 (Original): The device according to claim 24, wherein the sense amplifier amplifies the data read from the memory cell having either the first or second resistance based on the data held by the memory cell which has a resistance between the first and second resistances.

Claim 26 (Original): The device according to claim 25, wherein the sense amplifier identifies the data read from the memory cell having either the first or second resistance by a

magnitude with respect to the data read from the memory cell which has the resistance between the first and second resistances.

Claim 27 (Original): The device according to claim 23, further comprising:

a hold circuit which holds the value of the write current required to set the resistance of the magneto-resistive element of the memory cell to a value between the first and second resistances.

Claim 28 (Original): The device according to claim 23, further comprising:

a judgment circuit to judge whether or not the resistance of the magneto-resistive element of the memory cell is in a predetermined range between the first and second resistances; and

a control circuit to command the rewriting of the data with respect to the memory cell, when the resistance of the magneto-resistive element of the memory cell is not in the predetermined range as a result of judgment in the judgment circuit.

Claim 29 (Original): The device according to claim 28, wherein the control circuit controls the value of the current supplied by the driver circuit in accordance with a judgment result in the judgment circuit in commanding the rewriting.

Claim 30 (Canceled).

Claim 31 (Currently Amended): A control method of a semiconductor memory device comprising:

writing first data in a memory cell including a first magneto-resistive element, and writing second data in a reference cell including a second magneto-resistive element, the first magneto-resistive element of the memory cell in which the first data is written having either a first resistance or a second resistance smaller than the first resistance, the second magneto-resistive element of the reference cell in which the second data is written having a resistance between the first and second resistances;

precharging [[the]] a bit line;

reading the first and second data in the bit line from the memory cell and reference cell; and

amplifying the first data read in the bit line based on the second data,

wherein the memory cell and reference cell are disposed at an intersection of the bit line and word lines crossing at right angles to the bit line, and

an absolute value of the write current supplied to the bit line and word line in writing the second data in the reference cell is smaller than that of the write current supplied to the bit line and word line in reversing the data held in the memory cell to write the first data in the memory cell.

Claim 32 (Original): The method according to claim 31, wherein the second data is written into the reference cell at a die sort test time.

Claim 33 (Original): The method according to claim 31, further comprising:

holding information on a write current required in writing the second data in the reference cell in a hold circuit;

verifying whether or not the second data written in the reference cell is normal after writing the second data in the reference cell; and

reading the information held in the hold circuit and using the write current based on the information to write the second data in the reference cell again, when the second data is judged not to be normal as a result of the verification.

Claim 34 (Original): The method according to claim 31, further comprising:

verifying whether or not the resistance of the magneto-resistive element of the reference cell is in a predetermined range between the first and second resistances, after writing the second data in the reference cell; and

changing the value of the write current based on the verification result and writing the second data in the reference cell, when the resistance is judged not to be in the predetermined range as the result of the verification.

Claim 35 (Canceled).

Claim 36 (Currently Amended): The method according to claim [[35]] 31, wherein the write current supplied to the bit line and word line in writing the second data in the reference cell has a value between a minimum write current necessary for reversing the data held in the memory cell and a maximum write current permitted in non-reversing the data.

Claim 37 (New): The device according to claim 7, wherein the second memory cells are arranged at the intersection of any one bit line and word lines.

Claim 38 (New): The device according to claim 7, wherein the sense amplifier amplifies the data read from the first memory cell based on the data held by the second memory cell.

Claim 39 (New): The device according to claim 7, wherein the sense amplifier identifies the data read from the first memory cell by a magnitude with respect to the data read from the second memory cell.

Claim 40 (New): The device according to claim 7, further comprising:

a judgment circuit to judge whether or not the resistance of the magneto-resistive element of the second memory cell is in a predetermined range between the first and second resistances; and

a control circuit to command the rewriting of the data with respect to the second memory cell, when the resistance of the magneto-resistive element of the second memory cell is not in a predetermined range as a result of judgment in the judgment circuit.

Claim 41 (New): The device according to claim 7, wherein the control circuit controls the value of the current supplied by either one of the row driver and column driver in accordance with a judgment result in the judgment circuit in commanding the rewriting.